

What is claimed is:

1 1. An I/O circuit placement method for placing I/O
2 circuits included in a semiconductor device, comprising a step
3 of:

4 placing at least two rows of I/O circuits on a first side
5 of a chip, wherein each I/O circuit has a head
6 section and a tail section, the placement direction
7 of the head section and the tail section is
8 perpendicular to that of the I/O circuits in the
9 rows.

1 2. The placement method as claimed in claim 1 further
2 comprises a step of placing another row of I/O circuits on
3 a second side of the chip.

1 3. The placement method as claimed in claim 1, wherein
2 the head sections are oriented to the tail sections in the
3 adjacent rows.

1 4. The placement method as claimed in claim 1, wherein
2 the head sections are oriented to the head sections in the
3 adjacent rows.

1 5. The placement method as claimed in claim 1, wherein
2 a different number of I/O circuits are placed in different
3 rows.

1 6. A semiconductor device, comprising:
2 a chip; and
3 at least two rows of I/O circuits placed on a first side
4 of the chip, wherein each I/O circuit has a head

5 section and a tail section, the placement direction
6 of the head section and the tail section is
7 perpendicular to that of the I/O circuits in the
8 rows.

1 7. The semiconductor device as claimed in claim 6,
2 further comprising another row of I/O circuits placed on a
3 second side of the chip.

1 8. The semiconductor device as claimed in claim 6,
2 wherein the head sections are oriented to the tail sections
3 in the adjacent rows.

1 9. The semiconductor device as claimed in claim 6,
2 wherein the head sections are oriented to the head sections
3 in the adjacent rows.

1 10. The semiconductor device as claimed in claim 6,
2 wherein the tail sections are oriented to the tail sections
3 in the adjacent rows.

1 11. The semiconductor device as claimed in claim 6,
2 further comprising a core circuit region disposed on the chip,
3 wherein the rows of I/O circuits are disposed outside the core
4 circuit region and are at the periphery of the chip.

1 12. The semiconductor device as claimed in claim 6,
2 wherein the number of the I/O circuits placed in the different
3 rows is different.

1 13. A semiconductor device, comprising:
2 a chip;
3 a core circuit region disposed on the chip;

4 a loop of I/O circuits disposed at the periphery of the
5 chip and around the core circuit region; and
6 at least one row of I/O circuits disposed between the
7 loop of I/O circuits, wherein each I/O circuit has
8 a head section and a tail section, the placement
9 direction of the head section and the tail section
10 is perpendicular to that of the I/O circuits in the
11 loop or the row.

1 14. The semiconductor device as claimed in claim 13,
2 wherein the head sections are oriented to the tail sections
3 in the adjacent rows.

1 15. The semiconductor device as claimed in claim 13,
2 wherein the head sections are oriented to the head sections
3 in the adjacent rows.

1 16. The semiconductor device as claimed in claim 13,
2 wherein the tail sections are oriented to the tail sections
3 in the adjacent rows.